

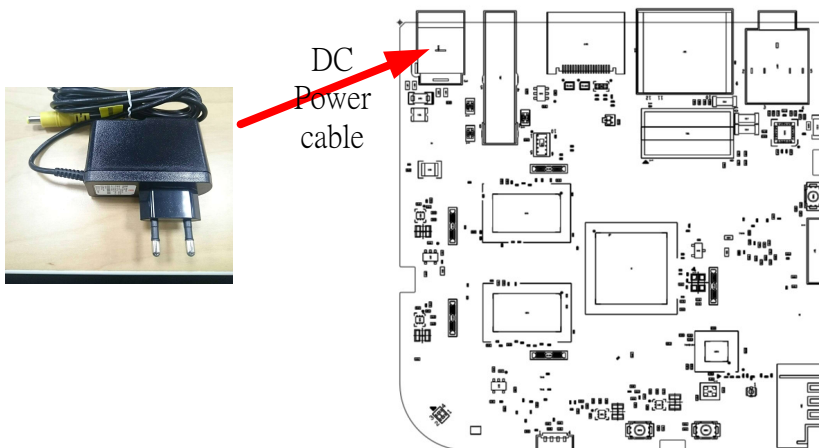
BFX-AT100

Hardware Unit Test Report

Power Sequence Test

Hardware version	FW version	Sample No.
V015	4.9.113 #29 Fri May 10 19:27:56 CST 2019 Build BFX_AT100-eng 9 PI 20190510 release-keys	S/N:

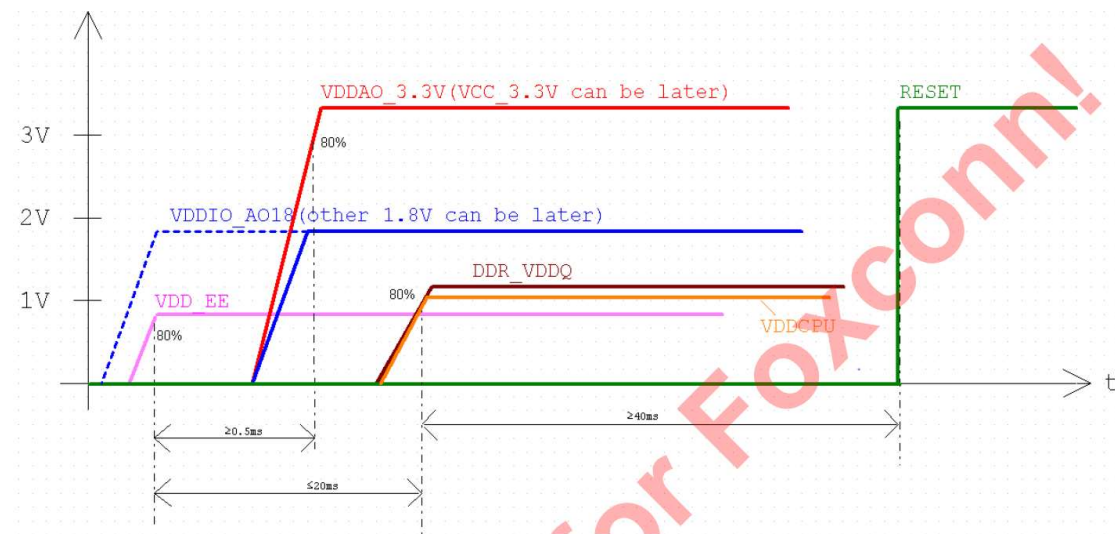
1. Power Test Setup



2. Test Condition

DC power: 5V 2A

3. Power on specification



Note:

- 1) All test value refer to 80% of typical power voltage.
- 2) VDDAO_3.3V & VCC3.3V should ramp up > 0.5ms later than VDD_EE.
- 3) All power sources should get stable within 20ms (except for DDR_VDDQ).
- 4) No sequence requirement between VDD18_AO and VDDEE. No sequence requirement between VDDCPU & DDR_VDDQ and other power source.
- 5) VDDIO_AO18 should ramps up earlier or at the same time with VDDAO_3.3V & VCC3.3V, VDDAO_3.3V & VCC3.3V should never be 2.5V higher than VDDIO_AO18.
- 6) In some designs, VDDCPU & VDD_EE are merged to VCC_CORE, the power on sequence should be same as VDD_EE.
- 7) RESET_n should keep low for at least 40ms after power up (except DDR_VDDQ).

Please refer to reference schematics.

4. Power on Result and Picture

Test Item	Test Result (ms)	Figure	Sequence	Pass/Fail
5V vs VDD_EE	4.464	Figure 1.	1	Pass
5V vs EMMC_VDDQ	4.984	Figure 2.	2	Pass
5V vs P1V8	5.04	Figure 3.	3	Pass
5V vs P2V5	5.124	Figure 4.	4	Pass
5V vs P3V3	5.128	Figure 5.	5	Pass
5V vs VDDCPU	5.476	Figure 6.	6	Pass
5V vs P1V2	5.504	Figure 7.	7	Pass
5V vs CPU_RST	396	Figure 8.	8	Pass
VDD_EE to P3V3 should ramp up >0.5ms	VDD_EE vs P3V3 =0.664			Pass

All power sources should get stable within 20ms (except for P1V2)	5V vs VDDCPU =5.476			Pass
CPU_RST should keep low for at least 40ms after power up (except P1V2).	VDDCPU vs CPU_RST =396			Pass

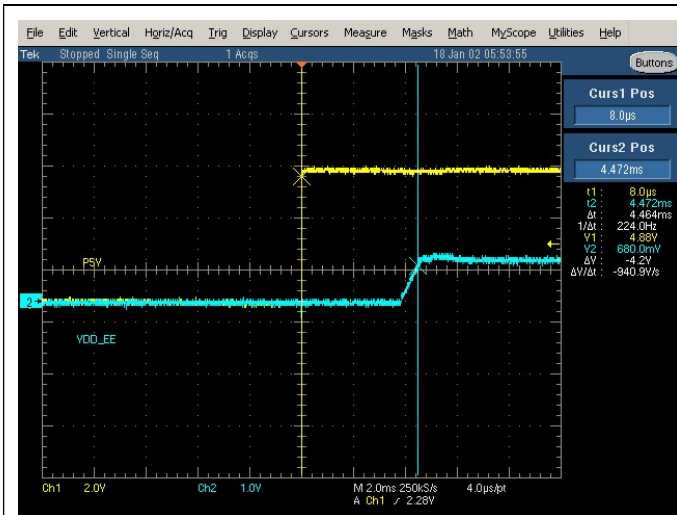


Fig. 1: 5V vs VDD_EE

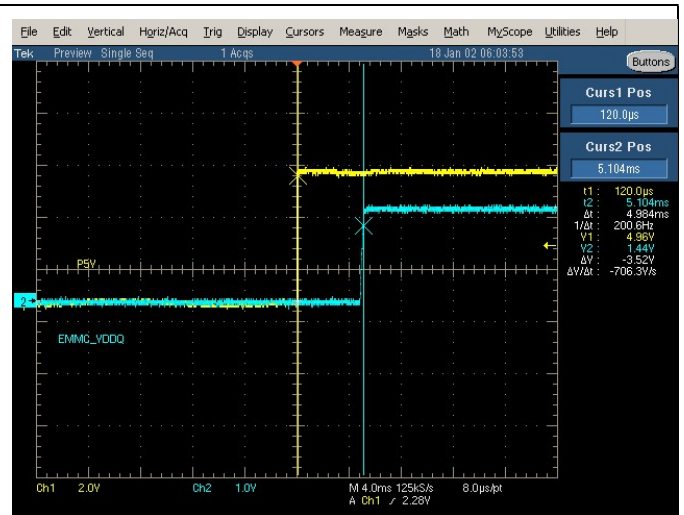


Fig. 2: 5V vs EMMC_VDDQ

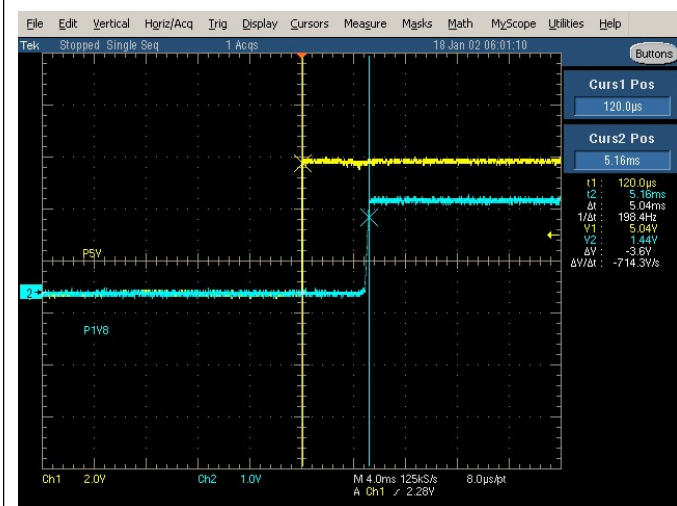


Fig. 3: P5V vs P1V8

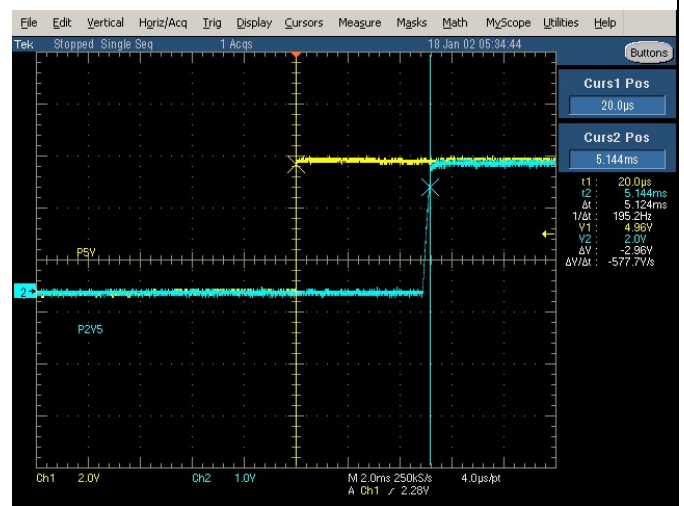


Fig. 4: P5V vs P2V5

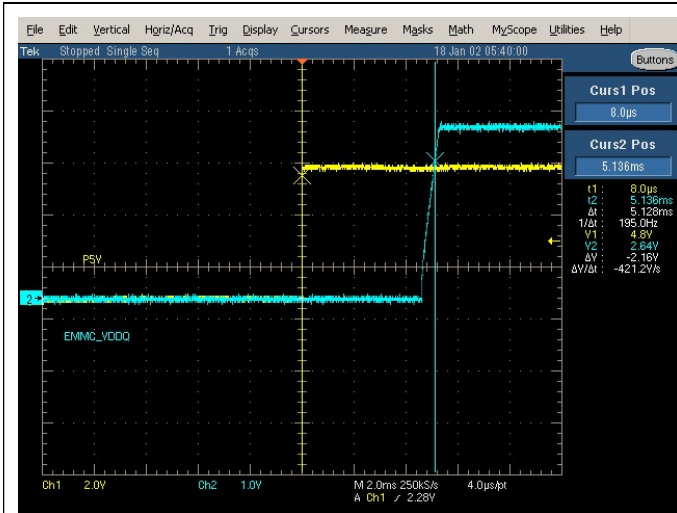


Fig. 5: P5V vs P3V3

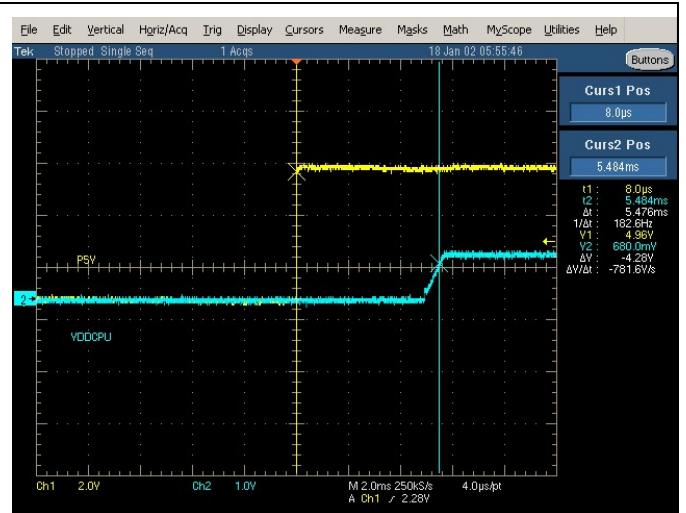


Fig. 6: P5V vs VDDCPU

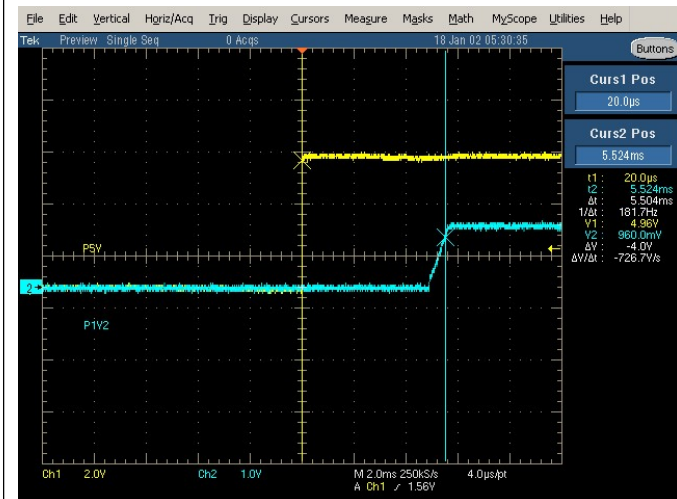


Fig. 7: P5V vs P1V2

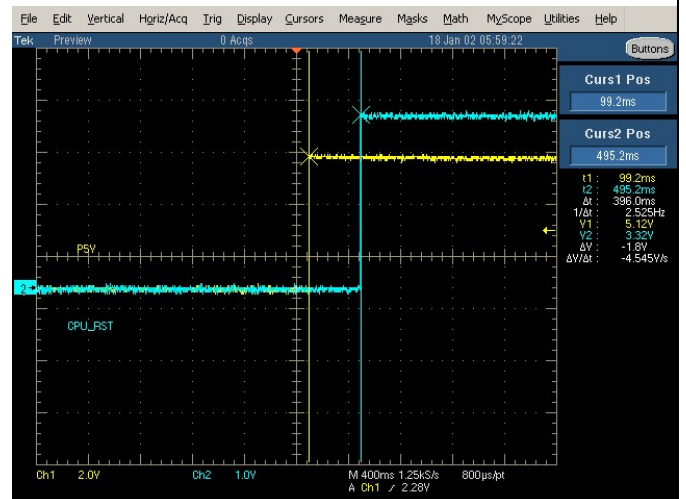


Fig. 8: P5V vs CPU_RST

5. Power off Picture

We can see that all power rail will down to 0V after power off.

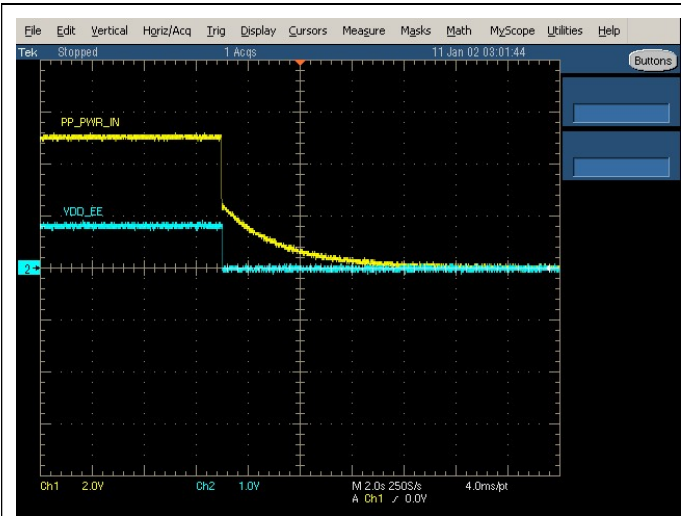


Fig. 1: 5V vs VDD_EE

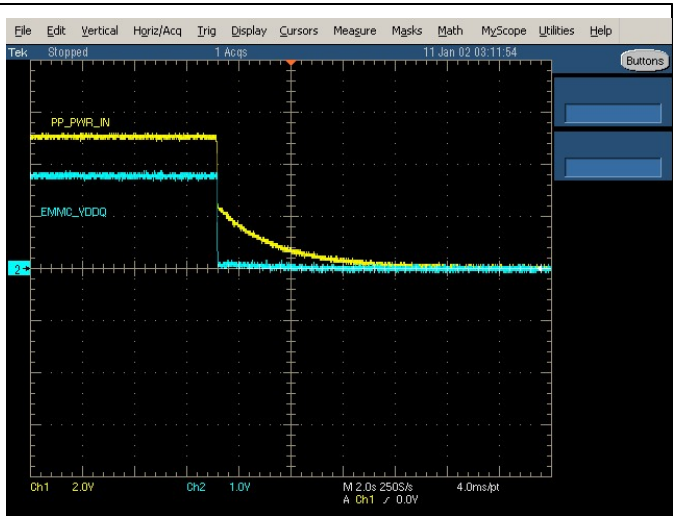


Fig. 2: 5V vs EMMC_VDDQ

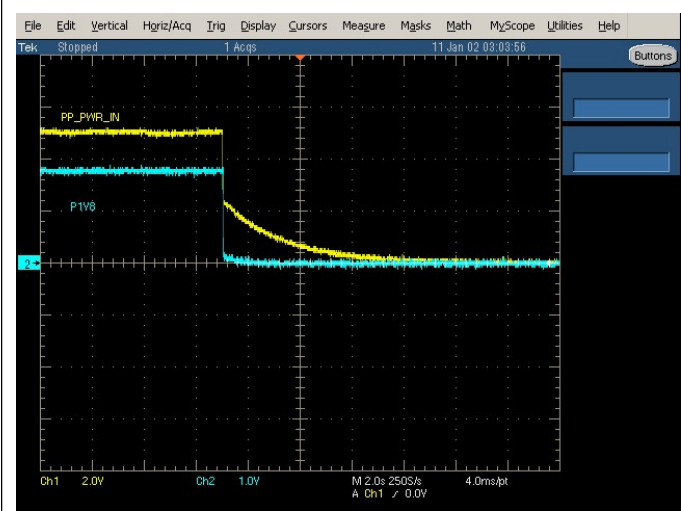


Fig. 3: P5V vs P1V8

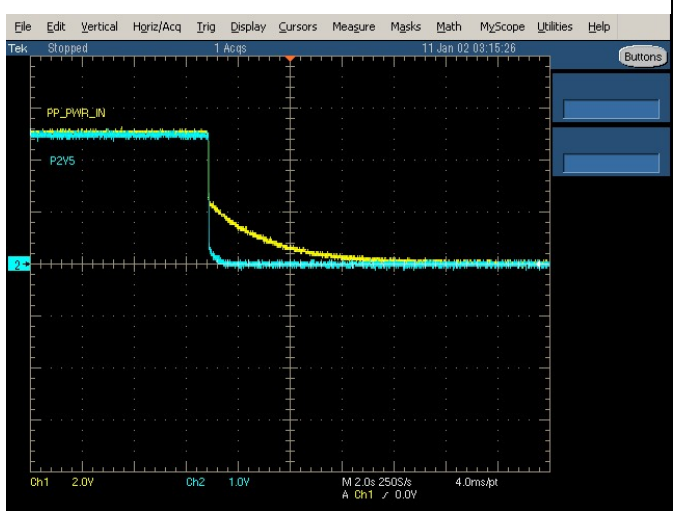


Fig. 4: P5V vs P2V5

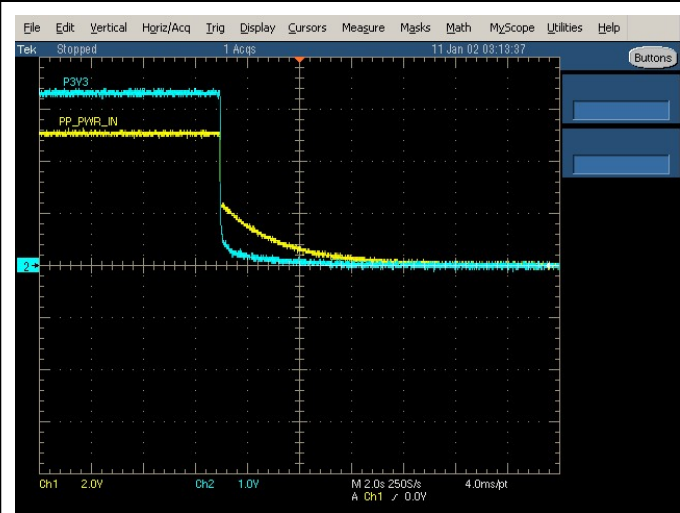


Fig. 5: P5V vs P3V3

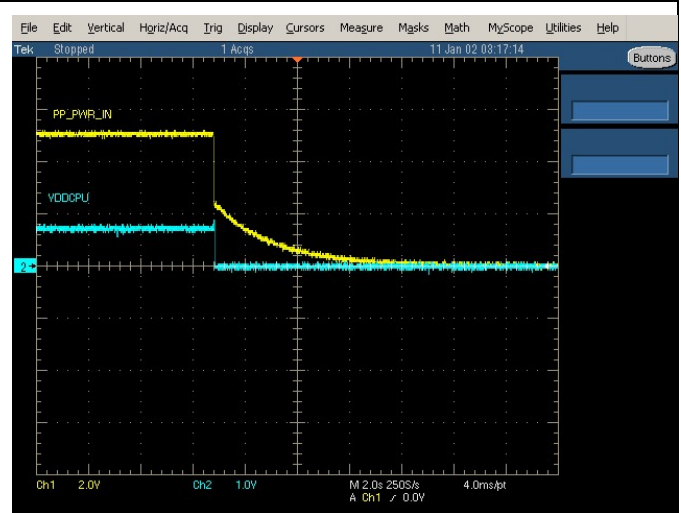


Fig. 6: P5V vs VDDCPU

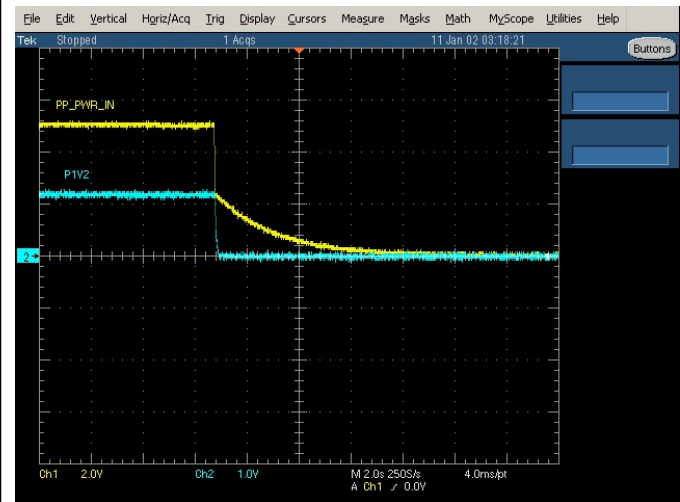


Fig. 7: P5V vs P1V2